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(71) Applicant: MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors: WANG, Ruoping; 3605 Steck Avenue, #2131, Austin, TX 78759 (US). GROBMAN, Warren, D.; 3205 Barker Hollow Pass, Austin, TX 78739 (US). CLINGAN, James, Lee, Jr.; 1317 Braided Rope Drive, Austin, TX 78727 (US).

(74) Agents: KOCH, William, E. et al.; Motorola, Inc., Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, TX 78729 (US).

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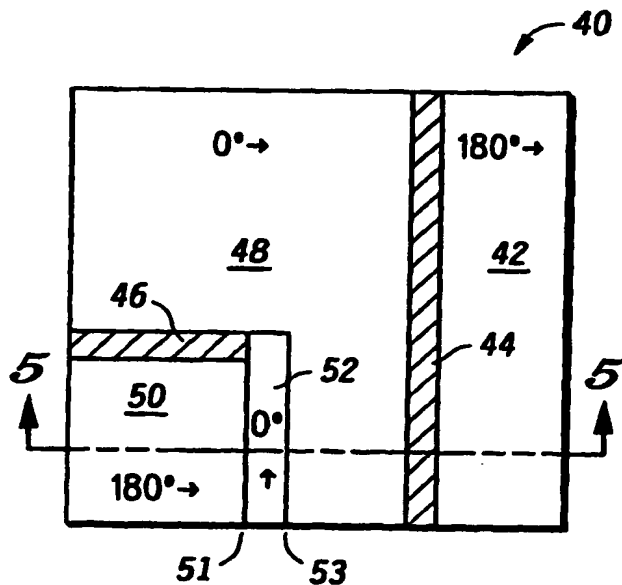
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(54) Title: MAKING AN INTEGRATED CIRCUIT USING POLARIZED LIGHT



(57) Abstract: A method and apparatus for making an integrated circuit takes advantage of both polarized and phase shifted light in order to achieve a fine feature. The feature on the integrated circuit is obtained by exposing a first region to light that has a first polarization state, exposing a second portion of the wafer to polarized light in the first polarization state but which is also phase shifted about 180 degrees. A region between the first and second region may be unexposed to light. The region between the first and the second region is the position of the fine feature. In areas where the first region and the second region need to be joined together but no feature is intended to be formed, there is a third region between the first and second regions which is exposed to polarized light that has a second polarization state which is orthogonal to that of the polarized light which exposes the first and second regions. The result is that the boundary between either the first or second region and the third region is fully exposed. Thus there is no artifact or extra feature formed in this boundary area between the first and second regions. Masks are made with corresponding regions to the first, second, and third regions so that the light in these polarized and phase shifted states is properly provided to the integrated circuit.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G03F1/00 G03F7/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G03F H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 5 541 026 A (MATSUMOTO KOICHI) 30 July 1996 (1996-07-30) column 11, line 66 -column 12, line 28 column 15, line 1 - line 5 column 16, line 50 -column 17, line 67 figures 6,7	1-54
X	US 5 677 755 A (FUKUDA KENICHIROU ET AL) 14 October 1997 (1997-10-14) column 15, line 53 -column 16, line 30 figures 25-27	1-54
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☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

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Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Heryet, C

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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